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Description

INDUCTOR FORMED BETWEEN TWO LAYOUT LAYERS

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to aninductor, and more specifically, to an inductor formed between two layout layers of a print circuit board (PCB) substrate.

[0003] 2. Description of the Prior Art

[0004] As wireless communication progresses, passive devices such as inductors, transformers, and capacitors widely used in circuit design for wireless communication are being integrated onto a chip. Inductors integrated onto the chip are applied to wireless integrated circuit design components such as low noise amplifiers (LNA), mixers, voltage controlled oscillators (VCO), and so on. However, the high power consumption of the chip may lowerthe quality level and increase the circuit design difficulties.

[0005] Please refer to Fig.1 which is a layout diagram illustrating a conventional planar inductor 10 according to the prior art. As shown in Fig.1, the planar inductor 10 is formed by a coil, which has two differential signal ends P1, P2and spirals inwards around a point O from the outer end P1 to the inner end P2 to form a necessary number of loops and then exits the plane from the P2 end.Because the coil of the planar inductor 10 cannot directly overlap itself, the overlapping section of the coil in Fig.1 is connected to another circuit board layer by a via plugconnected to the P2 end.A major drawback of the planar inductor 10 according to the prior is that the inductor consumes a large substrate area, increasing the cost and reducing the possibility of integrating it onto the chip.Reducing the distance of the inductor traces causes a narrower useful bandwidth. In addition, the quality factor of the planar inductor 10 and the resistance of the coil are inversely proportional. The longer coil, the larger the resistance, and therefore, increased energy dissipation of the planar inductor 10 reduces the quality factor and it become difficult to apply such an inductor in wireless integrated circuit design.

[0006] Please refer to Fig.2. Fig.2 is a layout diagram of a conventional two-level inductor 12 according to the prior art.

In order to reduce layout area, as shown in Fig.2, a two-level conductive coil is used to form the two-level inductor 12. The two-level inductor 12 includes two differential signal ends P1, P2 andspirals inwards around a line C from the P1 end to form a necessary number of loops.The coil is then connected to another circuit board layer by a via plug and then spiralsoutwards around the line C and ending atthe P2 end. It is worth mentioning that current flowing in the two layered coils is in the same direction, which increases the mutual inductance of the two-level inductor 12.In other words, the current flows into the end P1 from the outer ring to the inner ring in a clockwise direction, connects to the second layer by the via plug, and similarly flows clockwise from the inner ring to the outer ring ending at the P2 end. Although the two-level inductor 16 reduces layout area and increase mutual inductance between the two conductive coils when comparedwith the planar inductor 10,common mode noiseis not effectively reduced and results in a narrower utilized bandwidth.

[0007] As mentioned above, the conventional planar inductor 10 requires a larger layout area and increases cost. Additionally, a longer conductive coil causes a higher resistance, which lowers the quality level and results in the inductor

consuming more power. Although the two-level inductor 12 is capable of reducing layout area and improving the quality level, it is not able to reduce common mode noise and results in a narrower useful bandwidth.

SUMMARY OF INVENTION

[0008] It is therefore a primary object of the present invention to provide a printed circuit inductor in order to solve the problems mentioned above.

[0009] Briefly summarized, an inductor includes a first wiring layer, a second wiring layer, a first conductive trace, a second conductive trace, a third conductive trace, and a fourth conductive trace. The first conductive trace is on the first layout layer and the second conductive trace is on the second layout layer. The third conductive traceis parallel to the first conductive traceand is on the first wiring layer.The fourth conductive traceis parallel to the second conductive traceand is on the second wiring layer.The first end of the first conductive trace is connected to the first end of the second conductive trace through a first via plug. The second end of the second conductive trace is connected to the first end of the third conductive trace through a second via plug. The second end of the third conductive trace is connected to the first end of the fourth

conductive trace through a third via plug.

[0010] These and other objects of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0011] Fig.1 is a layout diagram illustrating a conventional planar inductor according to the prior art.

[0012] Fig.2 is a layout diagram of a conventional two-level inductor according to the prior art.

[0013] Fig.3 is a layout diagram illustrating aninductor according to the present invention.

[0014] Fig.4 is a sectional drawing along a cross-section 4-4' of the inductor shown in Fig.3.

[0015] Fig.5 to Fig.8 illustrate fouradditional types of inductors according to the present invention.

Detailed Description

[0016] Please refer to Fig.3 which is a layout diagram illustrating an inductor 14 according to the present invention. As shown in Fig.3, the inductor 14 includes a first wiring layer 16, a second wiring layer 18 which is formed under

the first wiring layer 16 and parallel to the first wiring layer 16,a first conductive trace 20 formed on the first wiring layer16, a second conductive trace 22 formed on the second wiring layer 18, a third conductive trace 24 formed on the first wiring layer 16 and parallel to the first conductive trace 20, a fourth conductive trace 26 formed on the second wiring layer 18 and parallel to the second conductive trace 22, a first via plug 28 which is perpendicular to the first conductive trace 20 and connected to a first end P1 of the first conductive trace 20 and a first end P2 of the second conductive trace 22, a second via plug 30 which is perpendicular to the second conductive trace 22 and connected to a second end P3 of the second conductive trace 22 and a first end P4 of the third conductive trace 24, and a third via plug 32 which is perpendicular to the third conductive trace 24 and connected to a second end P5 of the third conductive trace 24 and a first end P6 of the fourth conductive trace 26. The conductor 14 is formed by two separate coils spiraling along the Y-axis. The current flows into the P7 end, spiraling counterclockwise along the +Y direction toward the P8 end. The current could also flow into the P8 end, spiraling clockwise along the -Y direction toward the P7 end.

[0017] Please refer to Fig.4 which is a sectional drawing along a cross-section 4-4' of the inductor 14 shown in Fig.3. As shown in Fig.4, the conductor 14 is formed in a printed circuit board 34. The third conductive trace 24 is formed on the first wiring layer 16 and the second conductive trace 22 is formed on the second wiring layer 18. The second conductive trace 22 and the third conductive trace 24 are connected by the perpendicular second via plug 30. Similarly, the third via plug 32 is connected perpendicular to the third conductive trace 24.

[0018] In order to comply with different layout requirements, the inductor 14 can be of varied forms. Please refer to Fig.5 to Fig.8 which illustrate four additional types of inductors 50, 52, 54, 56 according to the present invention. In Fig.5 to Fig.8, conductive traces 38, shown as solid lines, are formed on the first wiring layer 16 and conductive traces 39, shown as broken lines, are formed on the second wiring layer 18. As shown in Fig.5 to Fig.8, the conductive traces 38 of the inductors 50, 52, 54, 56 on the first wiring layer 16 are parallel to each other and the conductive traces 39 on the second wiring layer 18 are also parallel to each other. In Fig.5 and Fig.6, the via plugs 42 are positioned along two parallel lines, in Fig.7 the via plugs

42 are aligned but are not positioned along two parallel lines, and in Fig.8the via plugs 42 are not aligned. Using these adaptations, the inductor14 can differ in various forms to comply with the layout design requirements.

[0019] The inductor according to the present invention can be composed of multilayered coils and manufactured by printed circuit board technology. The inductor includes a plurality of conductive layers, wherein each conductive layer includes a plurality of conductive traces arranged alternately, being isolated by a plurality of insulating layers. A plurality of via plugs perpendicular to the conductive tracesis used for connecting the traces between the different layers. The magnetic field generated by the inductor is in parallel with the conductive layers. All multilayered inductors having coils formed by conductive traces and via plugs are in the scope of the present invention.

[0020] The present invention provides a three-dimensional embedded inductor, which can be in various forms to comply with different layout requirements, to replace the conventional planar inductor. Moreover, the traces of the inductor are connected using via plugs to increase mutual induction of the traces. Therefore, the inductor according to the present invention requires shorter conductive lines to

achieve the same inductance as the conventional planar inductor. Thus, the inductor according to the present invention has a higher quality factor so that it can be applied widely in circuit design for high-frequency wireless communication.

[0021] In contrast to the prior art, the inductor according to the present invention requires a much smaller layout area so that the cost is reduced. Moreover, the traces of the inductor are connected using via plugs to increase mutual induction of the inductor for increasing the inductance per unit area, and therefore, the inductor according to the present invention requires shorter conductive lines to achieve the same inductance as the conventional planer inductor. Thus, the inductor according to the present invention has a higher quality factor so that it can be applied widely in circuit design for high-frequency wireless communication. Additionally, in the present invention, common mode noise is effectively reduced and the resonant frequency can be improved for increasing the utilized bandwidth.

[0022] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accord-

ingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.